

WHAT IS CLAIMED IS:

1 1. A processing core for executing instructions, comprising:
2 a first source register including a plurality of source fields;
3 a second source register including a plurality of result field select values
4 and a plurality of operation fields;
5 a multiplexer coupled to at least one of the source fields;
6 a destination register including a plurality of result fields; and
7 an operand processor coupled to at least one of the result fields, wherein
8 the operand processor and multiplexer operate upon at least one of the plurality of source
9 fields.

1 2. The processing core of claim 1, wherein:
2 the multiplexer includes a mux input, a select input and a mux output; and
3 the operand processor includes a processor input, a processor output and a
4 condition input.

1 3. The processing core for executing instructions of claim 2, wherein
2 the mux input is coupled to at least one of the source fields.

1 4. The processing core for executing instructions of claim 2, wherein
2 the select input is coupled to at least one of the result field select values.

1 5. The processing core for executing instructions of claim 2, wherein
2 the processor input is coupled to the mux output.

1 6. The processing core for executing instructions of claim 2, wherein
2 the condition input is coupled to at least one of the operation fields.

1 7. The processing core for executing instructions of claim 2, wherein
2 the processor output is coupled to at least one of the result fields.

1 8. The processing core for executing instructions of claim 1, wherein
2 the operand processor performs an operation selected from a group consisting of:
3 setting each bit from the source field low,
4 extension of a highest order bit of the source field to remaining bits,
5 bitwise inversion of the source field,

6 setting each bit of the source field high,
7 inversion of the highest order bit of the source field and extension of the
8 highest order bit to remaining bits,
9 bitwise reversion of the source field,
10 extension of the lowest order bit of the source field to remaining bits,
11 bitwise inversion and reversion of the source field, and
12 inversion of the lowest order bit of the source field and extension of the
13 inverted highest order bit to remaining bits.

1 9. The processing core for executing instructions of claim 1, wherein
2 the operand processor selectively stores a result in one of the result fields.

1 10. A method for performing an operation in a data processing
2 machine, the method comprising steps of:
3 selecting a source field from a source register having a first bit numbering;
4 manipulating the first source field to produce a result different from the
5 source field; and
6 storing the result in a result field of a destination register having a second
7 bit numbering, wherein:
8 the first and second bit numberings are identical,
9 the result originates from the source field having a first range
10 included in the first bit numbering,
11 the result field has a second range included in the second bit
12 numbering,
13 the first range is different from the second range; and
14 the manipulating and storing steps are associated with the same
15 instruction issue.

1 11. The method for performing the operation in the data processing
2 machine as recited in claim 10, further comprising a step of loading the source field from
3 the source register.

1 12. The method for performing the operation in the data processing
2 machine as recited in claim 10, wherein the manipulating step includes a step selected
3 from a group consisting of:

1 18. The method for performing the operation in the data processing
2 machine of claim 14, wherein the manipulation step includes a step selected from a group
3 consisting of:

4 setting each bit from the source field low,
5 extending a highest order bit of the source field to remaining bits,
6 bitwise inverting the source field,
7 setting each bit of the source field high,
8 inverting the highest order bit of the source field and extending the highest
9 order bit to remaining bits,
10 bitwise reverting the source field,
11 extending the lowest order bit of the source field to remaining bits,
12 bitwise inverting and reverting of the source field, and
13 inverting of the lowest order bit of the source field and extending the
14 inverted highest order bit to remaining bits.

1 19. The method for performing the operation in the data processing
2 machine of claim 14, wherein the loading, storing and manipulating steps are part of a
3 same instruction issue.